WHAT IS CLAIMED IS:

1. A hook switch circuit for use in a telephone line interface circuit, the circuit comprising:

a PNP transistor having a base, an emitter and a collector;

an NPN transistor having a base, an emitter and a collector, where the emitter of the NPN transistor is coupled to the base of the PNP transistor;

a first resistor coupled between the base of the NPN transistor and the emitter of the PNP transistor; and

a second resistor coupled between the base of the PNP transistor and the source of the PNP transistor.

2. The circuit of claim 1, the circuit further including a hook control circuit for receiving a hook control signal across an isolation barrier and, responsive thereto, generating an off-hook signal at an output of the hook control circuit, where the output of the hook control circuit is electrically coupled to the base of the NPN transistor.

3. The circuit of claim 2, the circuit further including:

a first metal-oxide semiconductor (MOS) transistor having a gate, a source and a drain, where the drain of the MOS transistor is electrically coupled to the base of the NPN transistor and the source of the MOS transistor is electrically coupled to a ground supply terminal; and

a first buffer having an input and an output, where the input of the first buffer is electrically coupled to the output of the hook control circuit and the output of the first buffer is coupled to the gate of the MOS transistor.

4. The circuit of claim 3, the circuit further including:

a first input/output pin configured to be coupled to a first terminal of a telephone line pair through a first high impedance resistor;

a second input/output pin configured to be coupled to a second terminal of a telephone line pair through a second high impedance resistor;

a polarity steering regenerative switch electrically coupled to the first and second input/output pins such that the switch receives power from the first and second terminals of the telephone line pair through the first and second high impedance resistors;

a current mirror electrically coupled to the polarity steering regenerative switch, where the current mirror is configured to generate an idle power supply voltage from a line

voltage obtained from the first and second terminals of the telephone line pair through the polarity steering regenerative switch; and

where the hook control circuit is configured to operate using the idle power supply voltage.

5. The circuit of claim 4, the circuit further including a second buffer having an input and an output, where the input of the second buffer is electrically coupled to one of the first and second input/output pins and the second buffer is configured to operate using power supplied by the polarity steering regenerative switch.

6. The circuit of claim 5, where the current mirror further includes an additional transistor configured to generate a current proportional to the line voltage at the first and second terminals of the telephone line pair.

7. The circuit of claim 4, the circuit further including:

a second MOS transistor having a gate, drain and source, where the gate of the second MOS transistor is electrically coupled to the output of the hook control circuit, the drain of the second MOS transistor is electrically coupled to the ground supply terminal, and the source of the second MOS transistor is electrically coupled to the current mirror; and

a third MOS transistor having a gate, drain and source and disposed between the output terminal of the hook control circuit and the base of the NPN transistor, where the gate of the third MOS transistor is electrically coupled to the drain of the second MOS transistor, the drain of the third MOS transistor is electrically coupled to the current mirror, and the source of the third MOS transistor is electrically coupled to the base of the NPN transistor such that generation of the off-hook signal results in a start signal that drives the base of the NPN transistor using current from the current mirror.

8. The circuit of claim 4, the circuit further including one of a transmit circuit and a receive circuit electrically coupled to one of the first and second input/output pins through a first isolation capacitor.

9. The circuit of claim 8, the circuit further including another one of the transmit circuit and the receive circuit electrically coupled to another one of the first and second input/output pins through a second isolation capacitor.

10. A telephone line interface circuit, the circuit comprising:

a first bipolar transistor having a base, emitter and collector, the emitter being electrically coupled to the telephone line;

a first resistor coupled between the base and the emitter of the first transistor;

a second bipolar transistor having a base, emitter and collector, the emitter of the second transistor being coupled to the base of the first transistor;

a second resistor coupled between the collector of the first transistor and the base of the second transistor;

a line side circuit including a hook switch control, the line side circuit having an off-hook power supply terminal coupled to the emitter of the second transistor, a hook switch control terminal coupled to the base of the second transistor, and first and second on-hook supply terminals for coupling to a TIP and RING of the telephone line, where the hook switch control is configured to operate in an on-hook state from power supplied from the TIP and RING through the first and second on-hook supply terminals, and where the hook switch control is configured to receive a hook signal having first and second states, where the hook switch control outputs current at the hook signal terminal responding to the off-hook state of the hook signal and outputs no current at the hook signal terminal responding to the on-hook state of the hook signal;

a third resistor having high impedance and coupled between the TIP of the telephone line and the first on-hook supply terminal; and

a fourth resistor having high impedance and coupled between the RING of the telephone line and the second on-hook supply terminal.

11. The telephone line interface circuit of claim 10, where the first and second transistors further comprise low-beta transistor devices.

12. The telephone line interface circuit of claim 10, where the line side circuit further includes a current mirror circuit interposed the first and second on-hook supply terminals and the hook switch control circuit, where the current mirror circuit is configured to produce an output current signal having a magnitude that is proportional to a line voltage at the TIP and RING of the telephone line.

13. The telephone line interface circuit of claim 12, where the line side circuit further includes a voltage to frequency converter for converting the output current signal to a frequency signal.

14. The telephone line interface circuit of claim 12, where the line side circuit further includes a polarity steering regenerative switch circuit interposed the first and second on-hook supply terminals and the current mirror circuit.

15. The telephone line interface circuit of claim 14, where the polarity steering regenerative switch circuit includes a buffer for generating a logic level line polarity signal.

16. The telephone line interface circuit of claim 12, the line interface circuit including:

a first isolation capacitor coupled between the first on-hook supply terminal and a modem side circuit; and

a second isolation capacitor coupled between the second on-hook supply terminal and a modem side circuit; and

where the line side circuit further includes:

a receiver circuit coupled to the first on-hook supply terminal and configured to receive a data signal from the TIP and RING and transmit the received data signal over the first isolation capacitor to the modem side circuit, and

a transmitter circuit coupled to the second on-hook supply terminal and configured to receive another data signal from the modem side circuit over the second isolation capacitor and transmit the another data signal to the TIP and RING.

17. A power circuit for a line powered telephone interface circuit, the power circuit comprising:

a first input/output pin configured to be coupled to a first terminal of a telephone line pair through a first high impedance resistor;

a second input/output pin configured to be coupled to a second terminal of a telephone line pair through a second high impedance resistor; and

a polarity steering regenerative switch electrically coupled to the first and second input/output pins such that the switch receives power from the first and second terminals of the telephone line pair through the first and second high impedance resistors.

18. The power circuit of claim 17, where the polarity steering regenerative switch comprises:

a first p-metal-oxide-semiconductor (PMOS) transistor having a gate, drain and source, where the drain of the first PMOS transistor is coupled to the first I/O pin and the gate of the first PMOS transistor is coupled to the second I/O pin; and

a second PMOS transistor having a gate, drain and source, where the drain of the second PMOS transistor is coupled to the second I/O pin, the gate of the second PMOS transistor is coupled to the first I/O pin, and the source of the second PMOS transistor is coupled to the source of the first PMOS transistor such that an idle supply voltage may be generated at the sources of the first and second PMOS transistors responsive to a voltage present at the first and second input/output pins.